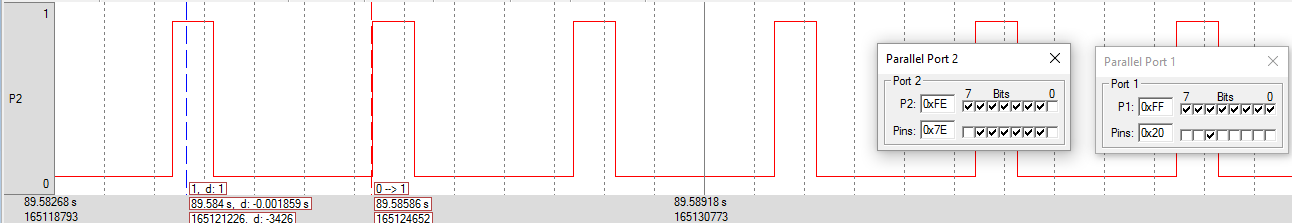
Initial Notes

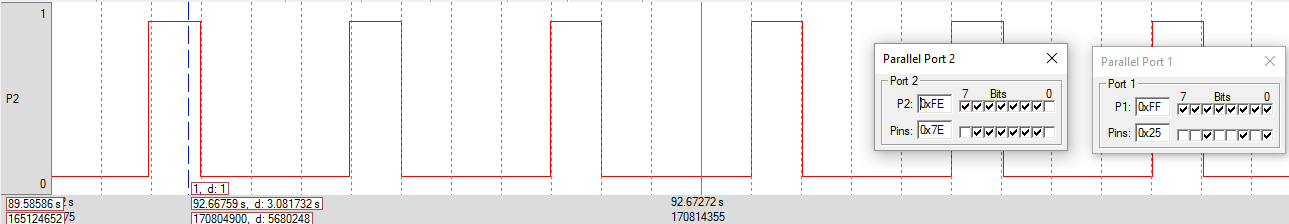
* Use Crystal value 22.1184 MHz
* AT89C51ED2 divides the crystal internally by 12
* Internal clock frequency = 22.1184MHz /12 = 1.8432 MHz
* 1 Clock cycle = 0.5425 µsec
* Calculations for required signal

|  |  |  |  |
| --- | --- | --- | --- |
| **Frequency Hz.** | **Time Ms.** | **Total No of Cycles** | **No of Cycles for 1% Duty Cycle** |
| **500** | **2,000** | **3,687** | **36.87** |

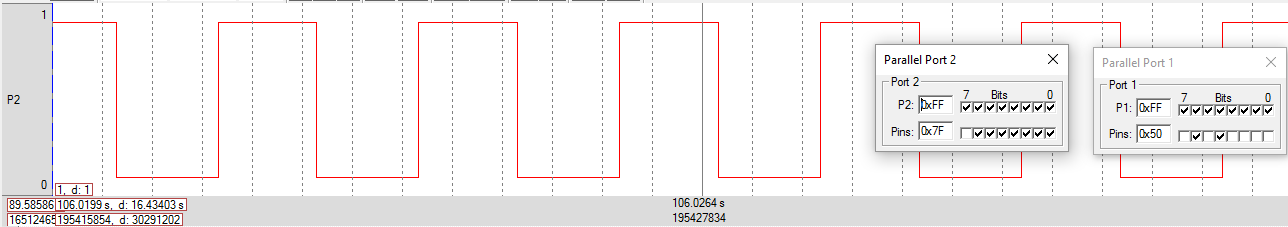
* We used the number of cycles required to generate 1% duty cycle to generate other duty cycles by multiplying that number with the input given
* Signal at 20% Duty Cycle



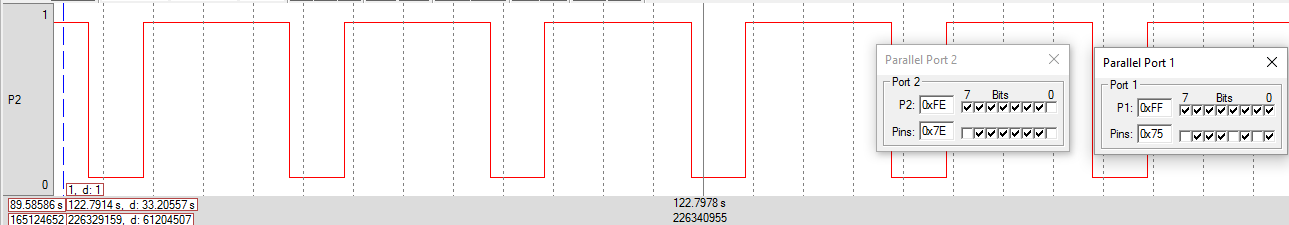
* Signal at 25% Duty Cycle



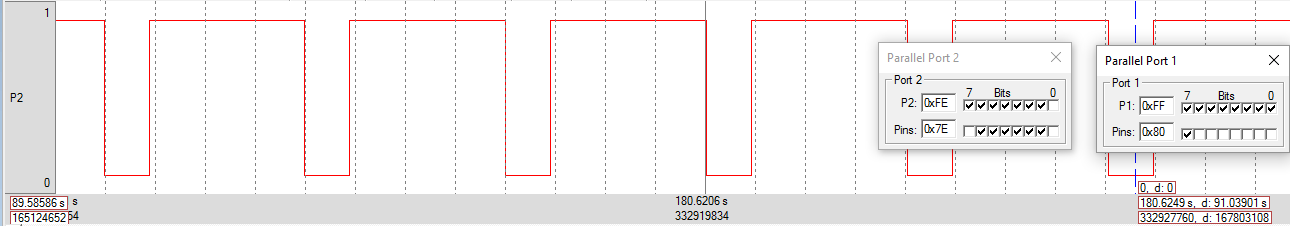
* Signal at 50% Duty Cycle



* Signal at 75% Duty Cycle



* Signal at 80% Duty Cycle



|  |  |
| --- | --- |
| **Duty Cycle** | **Expected Analog Voltage** |
| **20%** | **0.66v** |
| **25%** | **0.825v** |
| **50%** | **1.65v** |
| **75%** | **2.475v** |
| **80%** | **2.64v** |